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EXPERIMENTAL AND NUMERICAL STUDIES OF TRANSIENT HEAT  
TRANSFER IN ELECTRONICS PACKAGING

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EXPERIMENTAL AND NUMERICAL STUDIES OF  
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**EXPERIMENTAL AND NUMERICAL STUDIES OF TRANSIENT HEAT  
TRANSFER IN ELECTRONICS PACKAGING**

**by**

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## **LIST OF ABBREVIATION**

ANN	Artificial Neural Networks
AWE	Asymptotic Waveform Evaluation
BCI	Boundary Condition Independent
CFD	Computational Fluid Dynamics
CTE	Coefficient of Thermal Expansion
CTM	Compact Thermal Models
FEM	Finite Element Method
FHP	Flat Heat Pipe
FNM	Flow Network Modeling
GA	Genetic Algorithms
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
LMA	Low Melting Temperature Alloy
MPSoC	Multi-processor System-On-Chip
NetDAQ	Networked Data Acquisition Unit
PCB	Printed Circuit Board
PDR	Pitch-to-diameter Ratios
PSO	Particle Swarm Optimizers
QFP	Quad Flat Package
RC	Resistor-Capacitor
TIM	Thermal Interface Material
TSI	Through Silicon Interposer
TSV	Through Silicon Via

VAT	Volume Average Theory
VCTIM	Vertical Carbon Thermal Interface Material
VPS	Virtual Power Source
TDI	Transient Dual Interface

## LIST OF SYMBOLS

$C_p$	Specific heat J/KgK
$dT/dx$	Temperature gradient
$h$	Heat transfer coefficient W/m <sup>2</sup> .k
$k$	Thermal conductivity W/mK
$P$	Device power W
$Q$	Heat Flux W/m <sup>2</sup>
$q^n$	Convective heat flux w/m <sup>2</sup>
$R_{bd-a}$	Thermal resistance board to ambient C <sup>0</sup> /W
$R_{j-bd}$	Thermal resistance junction to board C <sup>0</sup> /W
$R_{c-p}$	Thermal resistance chip to package C <sup>0</sup> /W
$R_{jc}$	Thermal resistance-junction to chip C <sup>0</sup> /W
$R_{j-sink}$	Thermal resistance junction to sink C <sup>0</sup> /W
$R_{pa}$	Thermal resistance from package to ambient C <sup>0</sup> /W
$R_{sink-a}$	Thermal resistance sink to ambient C <sup>0</sup> /W
$T_a$	Ambient temperature °C
$T_{ball}$	Solder ball temperature °C
$T_j$	Junction temperature °C
$T_{max}$	Maximum temperature °C
$T_s$	Surface temperature °C
$T_{\infty}$	Fluid temperature
$u$	velocity in x direction m/s
$v$	velocity in y direction m/s
$\Theta_{sa}$	Thermal resistance- heat sink to ambient C <sub>0</sub> /W

$\Theta_{ja}$  Thermal resistance- junction to ambient  $C_0/W$

# **PENGAJIAN EKSPERIMEN DAN SIMULASI PEMINDAHAN HABLA FANA DALAM PAKAJ ELEKTRONIK**

## **ABSTRAK**

Permintaan bagi peranti mudah alih dan tablet adalah tinggi pada setiap masa dalam dekad yang lalu, perhatian yang amat menggalakkan telah ditumpu kepada bidang ini. Sesuatu kajian yang baru diperlukan dalam industri untuk mengiringi permintaan ini adalah untuk mengkaji ciri-ciri pemindahan haba sementara dan keadaan mantap, untuk memahami prestasi pemindahan haba yang memuaskan ke atas alat-alat ini, dan memastikan masa ujian haba untuk chip yang sesuai dengan output pengeluaran yang lebih baik. Fasa pertama kajian ini membentangkan keadaan mantap paksaan udara simulasi haba dengan lampiran penyebar haba untuk keadaan dengan pelbagai kuasa di dalam cip ( $0.5W-2.0W$ ). Model haba keadaan mantap telah berjaya dibangunkan dan dioptimumkan, dan kontur haba bagi setiap kuasa chip telah ditunjukkan. Model simulasi haba telah disahkan dengan pendekatan eksperimen dengan suhu simpangan dalam perbezaan peratusan pada 6.02%. Model haba yang disahkan telah dilanjutkan untuk mencirikan kesan daripada pelbagai aliran udara ke atas rintangan haba dari cip ke ambien. Ia menggunakan rangkaian rintangan haba dan simulasi secara holistik untuk analisis terma yang tepat. Keputusan menunjukkan bahawa rintangan haba dari cip ke ambien adalah fungsi aliran udara tetapi bukan kuasa cip, aliran udara yang lebih tinggi akan mengurangkan rintangan haba dari cip ke ambien. Dalam kajian ini, rintangan haba minimum diperolehi pada  $5.9^{\circ}C / W$  untuk aliran udara maksimum. Kajian seterusnya telah dilanjutkan kepada simulasi pemindahan haba sementara, dengan tujuan untuk memahami apakah sumber haba bantuan yang diperlukan untuk suhu simpangan mencapai  $70^{\circ}C$  dalam mod pemindahan haba sementara? Sumber haba bantuan ini adalah penting dalam

mengurangkan masa ujian chip. Pengetahuan yang mencukupi mengenai laluan pemindahan haba sementara telah ditunjukkan melalui penciptaan kontur haba dengan pelbagai sumber haba. Satu prototaip bantuan sumber haba telah berjaya dibina dan dikaji untuk membantu mengurangkan masa ujian haba untuk chip. Dan model pemindahan haba sementara juga telah disahkan dengan pendekatan eksperimen, keputusan simulasi pemindahan haba sementara dalam aspek masa yang diperolehi terletak dalam 11% daripada nilai eksperimen yang mengukur. Data menunjukkan ia memerlukan 22W sumber haba bantuan dan mengambil masa 69.65s untuk suhu simpangan mencapai 70<sup>0</sup>C daripada suhu bilik, in adalah satu pencapaian yang amat penting yang boleh digunakan dalam pengeshan chip. Kajian mengenai model pemindahan haba sementara disahkan juga dengan kesan pelbagai masa pemindahan haba sementara ( 15s - 75s ) dan sumber haba ( 7W - 27W ) untuk rintangan haba dari simpangan ke pateri bola. Rintangan haba dari cip ke pateri bola adalah fungsi masa sementara, di mana rintangan haba dari cip ke pateri bola meningkat dengan masa sementara; walau bagaimanapun, pada bila-bila masa tertentu rintangan haba tidak akan berubah dengan pelbagai sumber haba.

# **EXPERIMENTAL AND NUMERICAL STUDIES OF TRANSIENT HEAT TRANSFER IN ELECTRONICS PACKAGING**

## **ABSTRACT**

The demand for mobile and tablet devices is at all time high for the last decade, overwhelming attention has been paid to this field, the novelty studies that needed in industry to accompany this demand is to characterize the steady state and transient studies for satisfactory thermal performance on these devices, and ensuring reasonable thermal qualification time for chip and better production outputs. The part one of this study presents the steady state forced air thermal simulations with the attachment of heat spreader for various die power conditions (0.5W to 2.0W), the steady state thermal model has successfully been developed and optimized, and thermal contour for each die power was demonstrated. The simulated thermal model at steady state has been verified by thermocouple-measured junction temperature, with the maximum percentage difference at 6.02% only; the verified thermal model has been extended to characterize the thermal impacts of the various air flows on the resistance from die to the ambient. It utilizes heat path resistance network and simulation in a holistic manner for accurate thermal analysis. The results show that the heat path resistance from die to ambient is a function of air flow but not the die power, higher air flow will reduce the thermal resistance from die to ambient, and for this study the minimum thermal resistance obtained at  $5.9^{\circ}\text{C/W}$  for maximum air flow.

The part two of this study has been extended to transient heat transfer simulation, with the intention to understand what is the auxiliary heat source that required for the junction temperature to achieve  $70^{\circ}\text{C}$  at transient mode? The auxiliary heat source is